REMARKS/ARGUMENTS

Claims 1-3 and 5-42 were pending in the application. By this Amendment, claims 1 and 9 are being cancelled, claims 2, 3, 5-7, 10-18 and 21 are being amended and new claims 43-49 are being added, to advance the prosecution of the application. No new matter is involved.

In the Office Action, claims 1-3, 5, 6, 40 and 42 are rejected as unpatentable over Okumura in view of Sato. Claims 9-17, 20-26, 28-32 and 34-38 are rejected as unpatentable over Okumura in view of Yutaka and Sato. Claims 7, 8, 18, 19, 27, 33 and 39 are rejected as unpatentable over Okumura, Yutaka and Sato in view of Hamaka. Claim 41 is rejected as unpatentable over Okumura in view of Sato and U.S. Patent 5,517,543 of Schleupen. Claim 15 is rejected as unpatentable over Okumura, Yutaka and Sato, and Schleupen. These rejections are respectfully traversed.

Claim 1 is being cancelled, and claims 2, 3, 5, 6, 7 and 8 which depend, directly or indirectly, from claim 1 are being amended to depend from claim 42 which clearly distinguishes patentably over the art. None of the references disclose storage of a digital image signal having a size of two or more bits, so that claim 42 which recites such feature in accordance with the invention distinguishes patentably over the references. Similar comments apply to claims 2, 3 and 5-8 which depend, directly or indirectly, from claim 42.

Sato fails to disclose a structure in which a signal having a size of two or more bits is stored and a signal is selected corresponding to this number. In addition, the structure in which a signal having a size of two or more bits is stored and a signal is selected corresponding to the number of bits differs from the structures shown in Okumura and Yutaka. Moreover, in Okumura, because the output of the memory is directly applied to the liquid crystal, when the digital data

comprises a plurality of bits, it is not possible to output different voltage signals corresponding to different numbers of bits.

Similar comments apply to claim 41 which defines a structure similar to cancelled claim 1 plus a structure in which digital data is stored by an inverter and a capacitor, as shown in Fig. 4. This is not shown or suggested by any of the references.

Neither Okumura nor Sato disclose or suggest storage of a digital image signal using one or more inverters and capacitors. In addition, neither Okumura nor Sato disclose the necessity for such a structure. The Schleupen reference, cited as disclosing a capacitor and a buffer amplifier for storing image data, only discloses an internal structure of a shift register. There would be no motivation for applying such a circuit within a shift register as an element within each pixel. Accordingly, it would not be obvious to a person of ordinary skill in the art to employ the circuit structure of the shift register in each pixel.

Thus, claim 41 is submitted to clearly distinguish patentably over the references. Similar comments apply to new claims 43-48 which depend from claim 41 but which are otherwise identical to claims 2, 3, 5, 6, 7 and 8, respectively.

Claim 9 is being cancelled, and the limitations thereof are being added to claims 10 and 12. In addition, new claim 49 is being added so as to depend from claim 12 as so amended but which is otherwise identical to claim 10 in defining the combination of a display circuit selector and a data selector. Such claims clearly distinguish patentably over the references.

Sato does not have a structure for allowing storage and display of analog data. In Okumura, there is description and disclosure in Fig. 27 and lines 10-14 of column 27, as noted in the Office Action, that the memory circuit 1 (531) for storing digital data can store analog data. However, Okumura fails to disclose a structure

with both a first display circuit for selecting one display signal from among two or more display signals based on a digital signal stored in a storing circuit and for supplying the selected signal to a display element and a second display circuit which is separate from the first display circuit and having a storage capacitor for storing an analog image signal and for supplying the signal stored in the storage capacitor to the display element. In addition, there is no description or suggestion in the references that the structure therein has one or more of (a) a display circuit selector for selecting which of the display circuits the data to be displayed is written in, and (b) a data selector for selecting data from one of the display circuits and for outputting the selected data to the display element.

Moreover, neither Yutaka nor Sato disclose or suggest storage of digital data in each pixel and supply of both the digital and analog data to each pixel.

None of the cited references even alludes to the necessity for providing both a first display circuit for storing digital data and a second display circuit for storing analog data. However, and as now set forth in claims 10 and 12 as amended, either a selector for selecting to which of the two types of display circuits data is to be written or a selector for selecting data from among digital data and analog data output from the first and second display circuits is provided. None of the citations discloses such selectors, and, even when combined, the citations would not disclose or suggest the necessity for providing such selectors. Therefore claims 10 and 12 are submitted to clearly distinguish patentably over such references, in addition to claims 11, 13-19, 21, and new claim 49, which depend from and contain all of the limitations of such claims.

Regarding the rejection of claim 40, such claim defines structure in which one switching element reads a digital image signal of one bit from one drain line. In Sato, as described at lines 56-63 of column 11, two data lines (1-1a and 1-1b) are

employed for each pixel in order to write one digital data into a digital memory cell 100. Two signals of opposite phases are output onto these two data lines. In other words, in Sato, "one digital video signal" is written into the memory 100 using "two data lines". This structure completely differs from the structure described in claim 40. In addition, Okumura, et al. fails to disclose or suggest a signal selector which is operated based on data stored at the storing circuit for selecting an output signal from among two display signals and supplying the selected signal to the display element. Therefore, even when these citations are combined, the structure described in claim 40 cannot be obtained.

In conclusion, claims 2, 3, 5-8 and 10-49 are submitted to clearly distinguish patentably over the art for the reasons discussed above. Therefore, reconsideration and allowance are respectfully requested.

If for any reason the Examiner finds the application other than in condition for allowance, the Examiner is requested to call the undersigned attorney at the Los Angeles, California telephone number (213) 337-6846 to discuss the steps necessary for placing the application in condition for allowance.

If there are any fees due in connection with the filing of this response, please charge the fees to our Deposit Account No. 50-1314.

Respectfully submitted,
HOGAN & HARTSON L.L.P.

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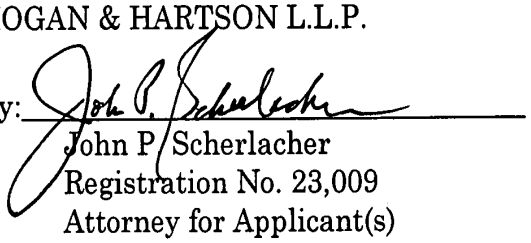
By: 
John P. Scherlacher
Registration No. 23,009
Attorney for Applicant(s)

500 South Grand Avenue, Suite 1900
Los Angeles, California 90071
Phone: 213-337-6700
Fax: 213-337-6701